

REMARKS

Claims 1 to 19 were pending in the application at the time of examination. Claims 1 to 19 stand rejected as obvious.

The Examiner objected to Figures 1 and 2 because these Figures included reference numerals not mentioned in the description. Applicant thanks the Examiner for the careful review of the specification and notes a typographical error in the objection because Figure 3 includes reference numeral 306 and 310 and not Figure 2.

Applicant has amended the specification to obtain correspondence between Figures 1 and 3 and the description. In particular, in the paragraph at page 12, lines 3 to 8 and in the paragraph at page 13, lines 1 to 8, the structures illustrated in Fig. 3 with reference numerals 310 and 306 are expressly called out. These amendments do not constitute new matter because in view of the information presented in Fig. 3 concerning the information carried on the structures with reference numerals 310 and 306, those of skill in the art would understand that the structures are address bus structures. Accordingly, the amendment only obtains the previously stated correspondence.

With respect to Fig. 1, paragraph 13 lines 19 to 28 was amended to reflect the specific structure denoted in Figure 1. In particular, memory 122 is shown as storing paged host adapter driver 120. Accordingly, the amendment does not constitute new matter and simply obtains correspondence between the drawing and the description.

In view of the amendments to the description, Applicant respectfully requests reconsideration and withdrawal of the objection to the drawings.

The other amendments to the description correct typographical errors. These amendments obtain consistency

within the description and correspondence between the description and the drawings.

Claims 1 to 5, and 11 to 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,659,690, hereinafter Stuber, in view of knowledge commonly known in the art as evidenced by the Free On-Line Dictionary of Computing.

The Examiner stated in part:

. . . The availability of only four active control blocks causes I/O bottlenecks in several situations. The Examiner takes Official Notice that the use of pages in a memory system that are accessed by splitting the address into a page number, as represented by the most significant bits of the address, and an offset within that page, as represented by the least significant bits of the address, in order to allow multiple items to be stored on a page is well known in the art. This is shown to have been well known in the art at the time the invention was made by The Free On-Line Dictionary of Computing (See entry for "paging"). Further, it is well known in the art that a pointer is an address, as evidenced by The Free On-Line Dictionary of Computing (See entry for "pointer").

Applicant respectfully traverses the use of Official Notice to the extent that the interpretation of the information noted fails to comply with the requirements of the MPEP. First, "paging" stated:

. . . A technique for increasing the memory space available by moving infrequently-used parts of a program's working memory from RAM to a secondary storage medium, usually disk. **The unit of transfer is called a page.** (Emphasis added)

. . . .

Paging allows the total memory requirements of all running tasks (possibly just one) to exceed the amount of physical memory,

Claim 1 recites that the plurality of pages is in the hardware I/O control block array. As used in Claim 1 and

described in the specification, paging does not allow the total memory requirements for the hardware control block array to exceed the amount of physical memory. Therefore, the rationale for paging as presented by the reference cited by the Examiner is unrelated to the rationale for paging as presented in the description. The description explicitly stated:

a size of an expanded SCB array 110 for a parallel SCSI host adapter 100 is increased so that the size of expanded SCB array 110 no longer limits the number of commands that can be queued to 255 commands. Herein, a SCB is an example of a hardware I/O control block. In this embodiment, expanded SCB array 110 is a memory array that is partitioned into a plurality of pages 111 0 to 111 N. (Emphasis added.)

Description, page 7, line 23 to 31.

Consequently, all the pages are in the physical memory as described and shown in the drawings and recited in Claim 1. Moreover, for an obviousness rejection, the MPEP directs:

DISCLOSED INHERENT PROPERTIES ARE PART OF "AS A WHOLE"
INQUIRY

"In determining whether the invention as a whole would have been obvious under 35 U.S.C. 103, we must first delineate the invention as a whole. **In delineating the invention as a whole, we look not only to the subject matter which is literally recited in the claim in question... but also to those properties of the subject matter which are inherent in the subject matter *and* are disclosed in the specification.** (Emphasis added).

MPEP §2141.02, 8th Edition, Rev. 1, p. 2100-122 (Feb. 2003)

As expressly recited in the Claims and as described in the description, the plurality of pages is included within the array. Accordingly, the motivation to use paging based upon

the rationale in the prior art, as quoted above, is unrelated to Applicant's invention as recited in Claim 1.

The MPEP further directs:

FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH PRIMA FACIE OBVIOUSNESS

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

MPEP §2143.01, 8th Edition, Rev. 1, p. 2100-126 (Feb. 2003).

The prior art does not suggest any reason to use paging because the pages are not being swapped in and out of the array based on usage to allow the total memory requirements to exceed the capacity of the array. In fact, using paging this way, teaches away from using paging in a situation where the total memory requirements are met as in Claim 1 because it is unnecessary to move the pages. Moreover, the MPEP further directs:

FACT THAT THE CLAIMED INVENTION IS WITHIN THE CAPABILITIES OF ONE OF ORDINARY SKILL IN THE ART IS NOT SUFFICIENT BY ITSELF TO ESTABLISH PRIMA FACIE OBVIOUSNESS

A statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references.

MPEP §2143.01, 8th Edition, Rev. 1, p. 2100-126 (Feb. 2003).

The motivation given by the Examiner for combining the three references was:

. . . in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory . . . , as well as to reduce the bottlenecks that can occur by having only four active control blocks.

The Examiner has cited no teaching in either the description or the claims (i) of main memory and secondary memory, (ii) of how to identify infrequently used control blocks, or (iii) of the moving of such control blocks based upon usage. Accordingly, the Examiner's motivation to combine the references is unrelated to Applicant's invention as recited in Claim 1.

Finally with respect to consideration of the invention as a whole including inherent properties disclosed in the disclosure, Applicant explicitly stated:

disclosure
With expanded SCB array 110, all SCSI target addresses can be supported at the same time. There is no restriction on how SCSI bus 180 is populated with target devices. No portion of array 110 is allocated to a particular SCSI target to the exclusion of other SCSI target devices. No special hardware assistance is required to access a SCB by a reconnecting target device. Sequencer 150 performs the search. In addition, no lookup tables are required to convert the tag from the reconnecting target device to a storage site for the corresponding SCB. Finally, very little time is required to locate the storage site using the tag as described above.

Description, page 15, line 26 to page 16, line 2.

None of these features, which are inherent in the invention as recited in Claim 1 and must be considered as quoted above from the MPEP, have anything to do with freeing up memory as postulated by the Examiner. None of these inherent properties has anything to do with moving an SCB between memories.

Accordingly, the motivation used by the Examiner, which is unrelated to Applicant's invention as recited in Claim 1, does not provide a sufficient basis to make the combination of references based upon the MPEP. Moreover, the MPEP stated that without the motivation, a prima facie obviousness rejection has not been established. Multiple reasons that the combination of references is inappropriate have been provided, but any one is sufficient to overcome the obviousness rejection. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 1.

With respect to the obviousness rejection of Claim 2, the Examiner relied upon the same motivation to combine the references as noted above. Therefore, the above comments with respect to Claim 1 and the combination of references are incorporated herein by reference. In addition, the portion of Stuber cited by the Examiner teaches nothing about addressing a location in a SCB array. In fact with only four slots, the SCB array of Stuber was simply walked to find the correct SCB. Determining whether a particular SCB in an array is the proper SCB for the reconnecting target as cited by the Examiner teaches or suggests nothing on how to address an SCB in the paged array as recited in Claim 2. Therefore, even if the combination of references were proper, Claim 2 distinguishes over the combination. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 2.

With respect to the obviousness rejection of Claims 3 to 5, the Examiner relied upon the same motivation to combine the references as noted above. Therefore, the above comments with respect to Claim 1 and the combination of references are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 3 to 5.

With respect to Claim 11, the Examiner used the same motivation to combine the same references as discussed in

Claim 1. However, as noted above and incorporated herein by reference, the hardware I/O control blocks are expressly stated to be "stored in a hardware I/O control block array." There is no recitation or description of moving blocks into and out of the array based upon use. Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 11.

With respect to the obviousness rejection of Claims 13 to 15, the Examiner relied upon the same motivation to combine the references as noted above for Claim 11. Therefore, the above comments with respect to Claim 11 and the combination of references are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 13 to 15.

With respect to Claim 16, the Examiner used the same motivation to combine the same references as discussed in Claim 1. However, as noted above and incorporated herein by reference, the hardware control blocks are expressly stated to be "in a memory." There is no recitation or description of moving blocks into and out of the memory based upon use. Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 16.

With respect to the obviousness rejection of Claims 17 to 18, the Examiner relied upon the same motivation to combine the references as noted above for Claim 16. Therefore, the above comments with respect to Claim 16 and the combination of references are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 17 to 18.

With respect to Claim 19, the Examiner used the same motivation to combine the same references as discussed in

Claim 1. However, as noted above and incorporated herein by reference, the expanded SCSI control block array includes the recited storage sites. There is no recitation or description of moving sites into and out of the array based upon use. Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. In addition, the Examiner rejected "hardware I/O control blocks" and not "SCSI control block storage sites." Accordingly, the very rejection shows that the references failed to suggest the structure recited. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 19.

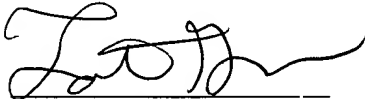
In the rejection of Claim 6 that includes the limitations of Claims 1, 3, 4, 5, and 6, the Examiner relied upon a combination of Stuber and Lysinger. Lysinger was cited only for a content addressable memory. Accordingly, assuming the combination is correct, this combination fails to suggest the paged array required for Claim 6. If the Examiner has incorporated the rejection of Claim 4, the above comments with respect to Claim 4 are incorporated herein by reference. Moreover, the Examiner has failed to show how Stuber would work with such a memory, because as noted above, the SCB array was walked. It requires a modification to Stuber that the Examiner has not addressed. Accordingly, the obviousness rejection of Claim 6 is not well founded for multiple reasons. Applicant respectfully requests reconsideration and withdrawal of the obviousness rejection of Claim 6.

Claims 7 to 10 depend from Claim 6. Therefore, assuming the additional information cited by the Examiner is properly combined, the additional information does not overcome the deficiency in the rejection with respect to Claims 1, 4 and 6 as noted above and incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 7 to 10.

Claims 1 to 19 remain in the application. For the foregoing reasons, Applicant(s) respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 19, 2004.



Attorney for Applicant(s)

March 19, 2004
Date of Signature

Respectfully submitted,



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